WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a chip mounting pad having a peripheral edge;

a semiconductor chip attached to the chip mounting pad;

a plurality of leads, each lead including an inner end and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end; and

at least one isolated ring structure disposed along the peripheral edge between the peripheral edge and the inner ends of the leads in spaced relation thereto, the ring structure being electrically connected to the semiconductor chip and the inner end of at least one of the leads.

2. The semiconductor package of Claim 1 wherein the inner end of each of the leads is vertically downset with respect to the distal end thereof a distance approximately equal to a thickness of the leads.

3. The semiconductor package of Claim 1 wherein:

the semiconductor chip includes a chip top surface;

the inner ends each include an inner end top surface;

and the inner end top surfaces are aligned with the chip top surface.

4. The semiconductor package of Claim 1 wherein:

the ring structure includes a ring top surface;

the inner ends each include an inner end top surface;

and the inner end top surfaces are aligned with

the ring top surface.

5. The semiconductor package of Claim 1 wherein each of the leads further includes a lead transition section disposed between the inner and distal ends thereof.

6. The semiconductor package of Claim 5 wherein the lead transition section is angularly disposed with respect to the distal end.

7. The semiconductor package of Claim 1 further comprising a sealing part encapsulating the inner ends of the leads.

8. A method of fabricating a semiconductor package, comprising the steps of:

a) providing a lead frame including:

a chip mounting pad having a peripheral edge;

a plurality of leads, each lead including an inner end and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto;

at least one isolated ring structure disposed along the peripheral edge between the peripheral edge and the inner ends of the leads in spaced relation thereto; and

at least one temporary connecting bar for connecting the ring structure to at least one of the chip mounting pad and the leads;

b) attaching a nonconductive connector to the ring structure and at least one of the leads for maintaining the ring structure in fixed relationship to the chip mounting pad and the leads;

c) removing the temporary connecting bar;

d) vertically downsetting the inner ends with respect to the distal ends;

e) attaching a semiconductor chip to the chip mounting pad;

f) electrically connecting the semiconductor chip to the ring structure; and

g) electrically connecting the ring structure to the inner end of at least one of the leads.

9. The method of Claim 8 wherein step d) includes vertically downsetting the distal ends with respect to the inner ends a distance approximately equal to a thickness of the leads.

10. The method of Claim 8 wherein the semiconductor chip includes a chip top surface and the inner ends each include an inner end top surface, and step d) includes aligning the inner end top surfaces with the chip top surface.

11. The method of Claim 8 wherein the ring structure includes a ring top surface and the inner ends each include an inner end top surface, and step d) includes aligning the inner end top surfaces wit the ring top surface.

12. The method of Claim 8 wherein step d) is accomplished via a die press operation.

13. The method of Claim 8 wherein each of the leads further includes a lead transition section disposed between the inner and distal ends thereof, and step d) includes vertically downsetting the inner ends with respect to the distal ends such that the lead transition sections are angularly disposed with respect to the distal ends.

14. The method of Claim 8 wherein step (a) comprises

forming the lead frame such that the temporary connecting bar extends between the ring structure and the chip mounting pad.

15. The method of Claim 8 wherein step (a) comprises forming the lead frame such that the temporary connecting bar extends between the ring structure and at least one of the leads.

16. The method of Claim 8 further comprising the step h) of encapsulating the inner ends of the leads with a sealing part of the semiconductor package.

17. A lead frame comprising:

a frame defining a central opening;

a chip mounting pad disposed within the opening and attached to the frame;

a plurality of leads attached to the frame and extending within the opening toward the chip mounting pad, each of the leads including an inner end disposed in spaced relation to and vertically downset from the chip mounting pad; and

at least one isolated ring structure extending between the chip mounting pad and the inner ends of the leads in spaced relation thereto.

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